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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/088,264	03/18/2002	Shin-Itsu Takehashi	OGOH:108	5130

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EXAMINER	
COLEMAN, WILLIAM D	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 03/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/088,264	TAKEHASHI ET AL.	
	Examiner	Art Unit	
	W. David Coleman	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19,24-26,28,29,32-39,41-46 and 52-54* is/are pending in the application.

4a) Of the above claim(s) *1-19,34-39,41-46 and 52-54* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *24-26,28,29,32 and 33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Group II invention, claims 1-23 and 34-54 in Paper filed December 22, 2003 is acknowledged. The traversal is on the ground(s) that that the subject matter of all of the claims would necessarily encompass a thorough and complete search for the subject matter of the non-elected claims. This is not found persuasive because they have acquired a separate status in the art because of their different classification, restriction for examination purposes as indicated is proper.

2. The requirement is still deemed proper and is therefore made FINAL.

Drawings

3. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "5" has been used to designate both polysilicon gate and source electrode. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

5. The drawings are objected to under 37 CFR 1.83(a) because they fail to show reference character "4" as described in the specification. Any structural detail that is essential for a proper

understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

6. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 24, 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al., U.S. Patent 6,4444,390 B1 in view of Zhang et al., U.S. Patent 6,255,705 B1.

9. Yamazaki discloses a semiconductor device substantially as claimed. See **FIGS. 1A-11**, where Yamazaki teaches the claimed product.

10. Pertaining to claim 24, Yamazaki teaches a top-gate LDD thin film transistor comprising: a gate electrode **206**, **207** and **208** having a thickness of not less than 100 nm and not greater than 250 nm (column 7, lines 58-62); and

insulating reaction product films **214**, **215** and **216** for coating both ends of the gate electrode in a channel direction, an insulating material each being 0.075 -- 0.5um long and thick

enough to function as a mask at a time of impurity injection (please note that silicon nitride films **214**, **215** and **216** have a thickness of 250 Å which is equivalent to 0.025 um). However, Yamazaki fails to teach the insulating reaction product films being oxide films of the gate electrode material. Zhang teaches an insulating reaction product films being oxide films of the gate electrode material. See **FIG. 1D**, where Zhang teaches an insulating material **117**, **118** and **119** that forms an oxide of the gate electrode material. In view of Zhang, it would have been obvious to one of ordinary skill in the art to incorporate the oxide material of Zhang into the semiconductor device of Yamazaki because silicon oxide film is to be formed into sidewall spacers (column 14, lines 1-5).

11. Pertaining to claim 25, Yamazaki teaches a top-gate LDD thin film transistor comprising:

a gate electrode **206**, **207** and **208** having a thickness of not less than 100 nm and not greater than 250 nm; and

insulating reaction product films **214**, **215** and **216** for coating both ends of the gate electrode in a channel direction, the insulating reaction product films being oxide films of the gate electrode material each being 0.075 -- 0.5um long and thick enough to function as a mask at a time of impurity injection, wherein a semiconductor layer directly below the insulating reaction product films comprises: an-offset region on a gate electrode side; and a low-concentration impurity-injected region on a side opposite to the gate electrode side. However, Yamazaki fails to teach the insulating reaction product films being oxide films of the gate electrode material. Zhang teaches an insulating reaction product films being oxide films of the gate electrode material. See **FIG. 1D**, where Zhang teaches an insulating material **117**, **118** and

119 that forms an oxide of the gate electrode material. In view of Zhang, it would have been obvious to one of ordinary skill in the art to incorporate the oxide material of Zhang into the semiconductor device of Yamazaki because silicon oxide film is to be formed into sidewall spacers (column 14, lines 1-5).

12. Pertaining to claim 26, Yamazaki teaches a top-gate LDD thin film transistor comprising: a gate electrode having a thickness of not less than 100 nm and not greater than 250 nm; and

insulating reaction product films for coating both ends of the gate electrode in a channel direction, the insulating reaction product films being oxide films of the gate electrode material each being 0.075 -- 0.5um long and thick enough to function as a mask at a time of impurity injection, wherein the LDD thin film transistor comprises a semiconductor layer located directly below the insulating reaction product films, the semiconductor layer having a low-concentration impurity intruded region due to heat diffusion or scattering on the gate electrode side; and a low-concentration impurity injected region on a side opposite to the gate electrode side. However, Yamazaki fails to teach the insulating reaction product films being oxide films of the gate electrode material. Zhang teaches an insulating reaction product films being oxide films of the gate electrode material. See **FIG. 1D**, where Zhang teaches an insulating material **117**, **118** and **119** that forms an oxide of the gate electrode material. In view of Zhang, it would have been obvious to one of ordinary skill in the art to incorporate the oxide material of Zhang into the semiconductor device of Yamazaki because silicon oxide film is to be formed into sidewall spacers (column 14, lines 1-5).

Claim Rejections - 35 USC § 102

13. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

14. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

15. Claims 28, 29 and 32 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamazaki et al., U.S. Patent 6,444,390 B1.

16. Pertaining 28, Yamazaki teaches a top-gate LDD thin film transistor comprising: a gate electrode having a thickness of not less than 100 nm and not greater than 250 nm; and a semiconductor layer having, at each end in a channel direction under the gate electrode, an offset region on the gate electrode side and a low-concentration impurity injected region on a side opposite to the gate electrode side in a range having a length of 0.075 -- 0.5um on both ends of the channel region provided under the gate electrode in the channel direction.

17. Pertaining to claim 29, Yamazaki teaches a top-gate LDD thin film transistor comprising: a gate electrode having a thickness of not less than 100 nm and not greater than 250 nm; and a semiconductor layer having, at each end in a channel direction under the gate electrode, a low-concentration impurity intruded regions due to heat diffusion or scattering on the gate electrode side and a low-concentration impurity injected region on a side opposite to the gate electrode side in a range having a length of 0.075 -- 0.5pm on both ends of the channel region provided under the gate electrode in the channel direction.

18. Pertaining to claim 32, Yamazaki teaches the top-gate LDD thin film transistor in accordance with claim 30, wherein the semiconductor layer is a polysilicon layer (column 4, line 23).

Claim Rejections - 35 USC § 103

19. Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al., U.S. Patent 6,444,390 B1 as applied to claims 28, 29 and 32 above, and further in view of Takemura U.S. Patent 6,534,832 B2.

20. Yamazaki discloses a semiconductor device substantially as claimed as discussed above. However, Yamazaki fails to teach the thin film transistor in accordance with claim 32, wherein the electric resistance in said low-concentration impurity injected region is 20 kΩ/□ and 100 k. kΩ/□. Takemura teaches wherein the electric resistance in said low-concentration impurity injected region is 20k kΩ/□ and 100 kΩ/□. In view of Takemura, it would have been obvious to one of ordinary skill in the art to incorporate the parameters of Takemura into the Yamazaki

semiconductor device because a lightly doped drain structure comprising impurities at a lower concentration, the sheet resistance falls in the claimed range (column 10, lines 5-10).

Conclusion

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 571-272-1856. The examiner can normally be reached on 9:00 AM-5:00 PM.

22. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

23. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

W. David Coleman
Primary Examiner
Art Unit 2823

WDC